FIG. 5 Shows the schematic structure of the CB-VDMOS—an example of the devices proposed by the inventor.

FIG. 6 Shows the schematic structure of the CB-VVMOS— an example of the devices proposed by the inventor.

FIG. 7 Shows the schematic structure of the CB-Diode—an example of the devices proposed by the inventor.

FIG. 8 Shows the schematic structure of the CB-Bipolar—an example of the devices proposed by the inventor.

FIG. 9 Shows the schematic structure of the CB-SIT—an example of the devices proposed by the inventor.

DETAILED DESCRIPTION OF THE INVENTION

By referring FIG. 1–FIG. 9, this invention can be further specified as follows.

FIG. 1 shows the RMOS, one of its fabrication process is:

(1) Epitaxial growth of an n^-(or p^-)-layer **5** on the n^+ (or p^+)-substrate **4**; (2) Diffusion of dopants to form a p^+ (or n^+)-layer **3** on the top; (3) Masked diffusion or ion-implant to form n^+ (or p^+)-regions **2**; (4) Selective trenching to make U-grooves and then growing gate-oxide **1** on the edges of the grooves: (5) Metal contacts—D.S.G.—formation.

FIG. 2 schematically shows a voltage sustaining structure using the CB-layer proposed by the inventor. One of its fabrication process is, (1) Epitaxial growth of an n^-(or p^-)-layer **5** on the n^+(or p^+)-substrate **4**; (2) Selective trenching on **5** to make very deep U-grooves, where the bottoms of the grooves just reach **4**; (3) Epitaxial growth of p(or n)-regions to fill up the grooves; (4) Epitaxial growth of a p^+(or n^+)-layer covering the CB-layer. The steps (2) and (3) can be replaced by a selective neutron transmutation doping (NTD), to transform local zones of the n(or p)-region into p(or n)-regions.

FIG. 3 shows the sectional view of some typical layouts of the CB-layer proposed by the inventor, where **6** denotes the N(or P)region, **7** denotes the P(or N)region, or vice versa.

FIG. 3-1 shows the interdigital layout.

FIG. 3-2 shows a hexagonal layout.

FIG. 3-3 shows the square mosaic layout.

FIG. 4 shows schematically the structure of the CB-RMOS, which is the most important example of the application of the CB-layer proposed by the inventor. An n(or p)-type epi-layer **5** is grown on the n^+(or p^+)-substrate **4**, then make **5** be a CB-layer according to the method stated in the specification about FIG. 2, where in **5**, **6** denotes n(or p)-region, **7** denotes p(or n)-region. Then, a p^+(or n^+)-region **3** is made on **5** by epitaxy or impurity diffusion, followed by a selective diffusion or ion-implant to make local n^+(or p^+)-regions **2** as the source. After that is done, a vertical trench is made, followed by a step of oxidation to make gate-oxide **1**. Finally, metal contacts G, S and D are made. The cell geometry can be any one of the interdigital, square, hexagonal, triangle and circle layouts.

FIG. 5 shows schematically the structure of the CB-VDMOS with a CB-layer proposed by the inventor. The fabrication process of this device is almost the same as that of the CB-RMOS (refer to FIG. 4), except that the step of forming the top trench is not used here. Also, dielectric films between **6** and **7** and/or between **4** and **7**, if any, are allowed.

FIG. 6 shows schematically the structure of the CB-VVMOS with a CB-layer proposed by the inventor. The fabrication process of this device is almost the same as that of the CB-RMOS (refer to FIG. 4), except that the top trenches formed are V-grooves, due to the <100> oriented wafer and a selective etching.

FIG. 7 shows schematically the structure of the high-voltage CB-Diode with a CB-layer proposed by the inventor. The CB-layer **5** is made on the n^+(or p^+)-substrate **4**, **6** and **7** in this figure denote two regions with different types of conduction (i.e. n-type and p-type). A p^+(or n^+)-layer is made on the top of the CB-layer by diffusion, or by ion-implantation or by epitaxy. Two metal contacts are made, one at the top side, the other at the bottom side.

FIG. 8 shows schematically the structure of the CB-Bipolar with a CB-layer proposed by the inventor. The fabrication process for making **4** and **5** (**6**, **7**) is the same as in the CB-diode (refer to FIG. 7). The outer-base p^+(or n^+)-region **9** and the inner-base p(or n)-region **10** are made successively by diffusion of impurities, followed by another diffusion (or ion-implant) to make the emitter n^+(or p^+)-region **11**. Finally, metal contacts for E, B and C are made.

FIG. 9 shows schematically the structure of the CB-SIT with a CB-layer proposed by the inventor. Although the buried-gate CB-SIT can also be made, only the example of the surface-gate CB-SIT is shown. The CB-layer is made as the same process as stated about FIG. 2. The p^+(or n^+)-regions **12** are made on the CB-layer as the gate, then, on the top layer the n^+(or p^+)-regions, **13** is used, is made, between the neighbor gates, as the cathode (or anode). Finally, metal contacts are made.

From FIG. 4 to FIG. 9 the existence of dielectric films between **4** and **7**, and/or between **6** and **7**, if any, are allowed.

I claim:

1. A semiconductor power device comprising:

a first contact layer of a first conductivity type;

a second contact layer of a second conductivity type; and

a voltage sustaining layer between said first and second contact layers, said voltage sustaining layer comprising first semiconductor regions of the first conductivity type and second semiconductor regions of a second conductivity type, said first and second semiconductor regions being alternately arranged, the voltage sustaining layer further comprising a thin dielectric layer located between one of said first semiconductor regions and one of said second semiconductor regions for isolating said one of said first semiconductor regions and said one of said second semiconductor regions, the first contact layer contacting said first semiconductor region forming a first interface, the second contact layer contacting the first and second semiconductor regions directly forming a second interface.

2. The semiconductor power device according to claim **1**, wherein the first contact layer is isolated from the second semiconductor regions by a second thin dielectric layer.

3. The semiconductor device of claim **1**, wherein said first and second interfaces are parallel to each other and perpendicular to the plane of the dielectric layer between said one of said first semiconductor regions and